REMARKS

First note regarding claims

Of the pending claims, claims 1-8 and 17-21 have been cancelled without prejudice. Applicant is not conceding that the subject matter of these claims is unpatentable, and reserves the right to reintroduce these claims in one or more subsequently filed continuing patent applications. Because claims 1-8 and 17-21 have been cancelled, their rejection is now moot, and Applicant does not discuss the rejection of these claims below.

Second note regarding claims

Of the pending claims remaining after the cancellation of claims 1-8 and 17-21, claims 9, 15, and 16 are independent claims. While claim 16 has been amended, claims 9 and 15 have not been amended in this response. Therefore, should the Examiner issue a rejection of claims 9 and 15 based on prior art different than the prior art used in the most recent office action, the next office action necessarily has to be non-final, and not final. MPEP sec. 706.07(a) states that "a second or any subsequent action on the merits in any application . . . *will not be made final* if it includes a rejection, *on newly cited art*, . . . of any claim not amended by applicant . . . in spite of the fact that other claims may have been amended to require newly cited art."

Prior art rejections as to claims 9-11 and 13-15

Claims 9 and 15 are independent claims, and claims 10-11 and 13 depend from claim 9. Claims 9-11 and 15 have been rejected under 35 USC 102(b) as being anticipated by Irie (6,038,644). Claim 13 has been rejected under 35 USC 103(a) as being unpatentable over Irie in view of Steely (2005/016043). Applicant respectfully submits that claims 9 and 15 as previously presented are patentable over Irie, such that claims 10-11 and 13 are patentable at least because they depend from a patentable base independent claim, claim 9.

In both claims 9 and 15, the claimed invention is limited to "selectively broadcasting the *cache miss* by the first node only to the sub-plurality of nodes." That is, what is selectively broadcast to the sub-plurality of nodes by the first node is a *cache miss*. Applicant respectfully submits that Irie does not disclose selectively broadcasting a *cache miss* in particular.

In Irie, a *coherent request* concerning data is selectively broadcast to a sub-plurality of nodes (see, e.g., col. 4, ll. 30-45), not a *cache miss* in contradistinction to the claimed invention. A *coherent request* as used in Irie is not a cache miss, however. For instance, Irie says the following:

> When the miss of the cache memory 300 is detected by the hit detect logic 352 in the cache control unit 350 (FIG. 3), the judge result of the hit check is notified [sic] to the cache status control logic 354 through line 3520. *The cache status control logic 354 responds to this notification, and generates a coherent processing request* in the register 360 (FIG. 4). . . . The coherent processing request requests the other processor units to execute processing for maintenance of coherency concerning the data of the address designated by the previously executed memory access instruction.
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> . . . .
>
> When a coherent processing request is transferred to other plural processor units, the present embodiment controls its destination so that it does not transfer the request to all other processor units but only to part of the processor units which are likely to have cached the data designated by the request.

(Col. 7, ll. 44-56; col. 8, ll. 17-21). Thus, in Irie, notification of a cache miss is sent to the status control logic. The status control logic in response to this notification generates a coherent processing request, which is transferred to other nodes (e.g., processor units). The cache miss itself is *not* transferred to other nodes, in contradistinction to the claimed invention, but rather a coherent processing request is generated in response to the cache miss and it is the coherent processing request that is transferred to other nodes in Irie.

Therefore, Irie does not anticipate the claimed invention. The claimed invention is limited to selectively broadcasting a *cache miss* to other nodes. By comparison, Irie discloses selectively

broadcasting a *coherent processing request* to other nodes, where this coherent processing request is generate in response to receiving notification of a cache miss.

Prior art rejections of claims 12 and 16

Claim 12 is a dependent claim, depending from claim 11, and claim 16 is an independent claim. Claim 12 has been rejected under 35 USC 103(a) as being unpatentable over Irie in view of Steely. Claim 16 has been rejected under 35 USC 102(b) as being anticipated by Irie. Claim 12 has not been amended herein, while claim 16 has been amended so that in relevant part it discloses the same claim language as claim 12. Applicant respectfully submits that claim 12 as previously presented and claim 16 as presently amended are patentable over Irie in view of Steely. (Of course, claim 12 is also patentable at least because it depends from a patentable base independent claim, claim 11, as has been discussed above.)

Claims 12 and 16 are limited to determining whether the cache miss should be selectively broadcast to the sub-plurality of nodes by at least determining whether the first node – from which the cache miss is selectively broadcast – is a *home node* for the memory unit to which the cache miss in question relates. That is, at least part of determining whether a first node should selectively broadcast a cache miss to a sub-plurality of other nodes is determining whether the first node itself is the home node for the memory unit to which the cache miss relates. Applicant respectfully submits that Irie in view of Steely does not suggest this aspect of the invention.

Irie in view of Steely rather just *at best* suggests that a first node should selectively broadcast a cache miss *to a sub-plurality of nodes including the home node* for the memory unit to which the cache miss relates, where the first node is not the home node. For example, Irie in view of Steely discloses that a "processor 117 . . . generates two parallel requests for the desired cache line, a first request . . . to the home node 180 and a second request . . . to any predicted target processors" (Steely, para. [0055]). Note that the processor 117 under discussion is not

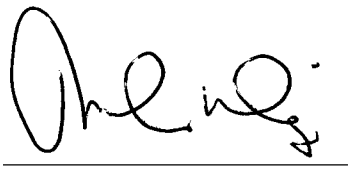
part of the home node 180, but rather is part of a "first node" – to use the parlance of the claim language – that is a node other than the home node (see FIG. 3 of Steely).

As such, Irie in view of Steely does not suggest that a first node is to determine whether a cache miss should be selectively broadcast from the first node to a sub-plurality of nodes *based on whether the first node is itself the home node for the memory unit to which the cache miss in question relates*, as in the claimed invention. Rather, Irie in view of Steely suggests that *at best* a first node is to selectively broadcast a cache miss from the first node *to the home node* for the memory unit to which the cache miss in question relates, *where the first node is necessarily not the home node*. Therefore, Irie in view of Steely does not render the claimed invention *prima facie* obvious and unpatentable.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicant's representative, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For the reasons discussed above, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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